a patterned [oxide] layer disposed over the substrate;

a layer of undoped silicate glass disposed over the patterned [oxide] layer;

a layer of borophosphorous silicate glass over the layer of undoped silicate glass;

a first planarized layer of plasma-enhanced tetraethyl orthosilicate over at least a portion of the layer of the borophosphorous silicate glass, and not overlaying at least a portion of the borophosphorous silicate glass layer; and

a second layer of plasma-enhanced tetraethyl orthosilicate overlaying the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with [at least a] the portion of the borophosphorous silicate glass [region] layer, not overlaid by the first layer of plasma-enhanced tetraethyl orthosilicate, the layers of the undoped silicate glass, borophosphorous silicate glass, planarized plasma-enhanced tetraethyl orthosilicate and second plasma-enhanced tetraethyl orthosilicate layer together forming a pre-metal dielectric stack.

4. (Amended) The structure of claim 3 wherein a combined thickness of the [oxide] patterned layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the second layer of plasma-enhanced tetraethyl orthosilicate is less than approximately [15k] 15,000 angstroms.

6. (Amended) An integrated circuit, comprising:

a substrate;

a dielectric layer disposed on the substrate;

a layer of undoped silicate glass disposed on the dielectric layer;

an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass;

a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, the planar dielectric layer directly overlaying at least a portion of the borophosphorous silicate glass and leaving exposed so as to not directly overlay at least a portion of the borophosphorous silicate glass; and